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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/424,544
Filing Date: November 24, 1999
Appellant(s): INO ET AL.

Ronald P. Kananen
(Registration Number 24,104)
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed *2 December 2008* appealing from the Office action mailed *28 May 2008*.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

4,825,203	***Takeda et al.***	4-1989
5,440,304	***Hirai***	8-1995
5,426,447	***Lee***	6-1995
4,745,406	***Hayashi et al.***	5-1988

(9) Grounds of Rejection

The following grounds of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102 / 103

1. Claims 25-29, 31, 37, 43-48, and 71-78 are rejected under 35 U.S.C. 102(b) as anticipated by ***Takeda et al (US 4,825,203 A)***.

2. Claims 25-29, 31, 37, 43-48, and 71-78 are rejected under 35 U.S.C. 102(b) as anticipated by ***Hirai (US 5,440,304 A)***.

3. In the alternative, claims 25-29, 31, 37, 43-48, and 71-78 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Takeda et al (US 4,825,203 A)*** in view of ***Hirai (US 5,440,304 A)***.

Regarding claim 25, ***Takeda*** discloses a liquid crystal display [*Fig. 2*] comprising:

a display portion [*Fig. 2: liquid crystal color display panel 11*], said display portion having

a plurality of gate lines [*Fig. 2: row electrodes 11-a*],

a plurality of signal lines [*Fig. 2: column electrodes 11-b*] and

a plurality of pixels [*Fig. 2: RGB display picture elements 11-c*],

a pixel of said plurality of pixels being located at an intersection of a gate line of said plurality of gate lines and a signal line of said plurality of signal lines (*Fig. 2*); and

a plurality of driver circuits (*wherein the total column electrode drive circuit [Fig. 2: 13] is made up by a plurality of single column driver circuits, each single column driver circuit comprising:*

a shift register [Fig. 1(A): 31],

an output terminal [Fig. 1(A): q],

three AND gate circuits [Fig. 1(A): 37],

three analog switches [Fig. 1(A): 32],

a first condenser [Fig. 1(A): 33],

another analog switch [Fig. 1(A): 34],

a second condenser [Fig. 1(A): 35],

an output buffer [Fig. 1(A): 36], and

a column electrode output terminal [Fig. 1(A): Q]),

said plurality of driver circuits including

at least one general driver circuit (*e.g., an arbitrary grouping of the first three leftmost column driver circuits [Fig. 1(A): (q_1 to Q_1) + (q_2 to Q_2) + (q_3 to Q_3)]*) and

one remainder driver circuit (*e.g., an arbitrary grouping of the last two rightmost column driver circuits [Fig. 1(A): (q_{N-1} to Q_{N-1}) + (q_N to Q_N)]*),

each said at least one general driver circuit having

a general driver horizontal shift register circuit [*Fig. 1(A): shift register 31 at output terminals q_{1-3}*] and

a plurality of general driver circuit output terminals [*Fig. 1(A): output terminals Q_{1-3} from output buffers 36_{1-3}*],

a general driver circuit output terminal of said plurality of general driver circuit output terminals providing a signal potential ("*a signal corresponding to the display pattern*") to one of said plurality of signal lines (*wherein output terminals [Fig. 1(A): Q_{1-3}] from output buffers [Fig. 1(A): 36_{1-3}] output display signals to the first three leftmost column electrode lines [Fig. 2: column electrodes 11-b])*,

said remainder driver circuit having

a remainder driver horizontal shift register circuit [*Fig. 1(A): shift register 31 at output terminals q_{N-1}, q_N*] and

a plurality of remainder driver circuit output terminals [*Fig. 1(A): output terminals Q_{N-1}, Q_N from output buffers 36_{N-1}, 36_N*],

a remainder driver circuit output terminal of said plurality of remainder driver circuit output terminals providing another signal potential to another of said plurality of signal lines (*wherein output terminals [Fig. 1(A): Q_{N-1}, Q_N] from output buffers [Fig. 1(A): 36_{N-1}, 36_N]*

output display signals to the last two rightmost column electrode lines [Fig. 2: column electrodes 11-b]),

the quantity [*2*] of said remainder driver circuit output terminals [*Fig. 1(A): output terminals Q_{N-1}, Q_N*] being defined as (S - (OP * (DC-1))),

"S" being the quantity [*5*] of said plurality of signal lines [*Fig. 1(A):For simplicity's sake set the number of column signal lines at N = 5. However please note, the number of column signal lines could be set as high as desired. Simply increase the number of general driver circuit output terminals accordingly and the instantly claimed equation will still work.*],

"OP" being the quantity [*3*] of said general driver circuit output terminals [*Fig. 1(A): output terminals Q_{1-3}*], and

"DC" being the quantity [*2*] of said plurality of driver circuits [*Fig. 1(A): output terminals Q_{N-1}, Q_N*], and

said quantity [*3*] of said general driver circuit output terminals being different than said quantity [*2*] of said remainder driver circuit output terminals [*Fig. 1(A) and Column 4, Lines 22-68. Wherein S - (OP * (DC-1)) = 5 - (3 * (2-1)) = 5 - (3 * 1) = 5 - 3 = 2 = the quantity of remainder driver circuit output terminals = 2*].

Claim 25 is claiming little more than a display having two driver circuits (*one driver circuit having more outputs than another*).

It is the examiner's contention that such a broad claim would read on most any display having five or more line drivers -- which can be arbitrarily divided into two driver groups/circuits (*with one driver group/circuit having more outputs than the other*).

The instant claim nowhere expressly specifies that the general driver horizontal shift register circuit and the remainder driver horizontal shift register circuit must be different and distinct from one another.

Therefore, an artisan would reasonably expect that a single generic shift register circuit may be shared by both the general driver horizontal shift register circuit and the remainder driver horizontal shift register circuit of the instant invention.

Furthermore, the examiner takes official notice that one having ordinary skill in the art at the time of invention would recognize that ***Takeda's*** shift register circuit [*Fig. 1(A): 31*] is conventionally comprised by a series of distinct flip-flops set up in a linear fashion which have their inputs and outputs connected together in such a way that the data [*Fig. 1(A): D*] are shifted down the line [*Fig. 1(A): from q_1 to q_N*] when the circuit is activated [*Fig. 1(A): via clock signal Φ*].

In such a manner, ***Takeda's*** shift register circuit [*Fig. 1(A): 31*] would conventionally have a first set of flip-flops provided for the general driver circuitry [*Fig. 1(A): outputting at q_1,*

q_2, and q_3] and a subsequent second set of flip-lops provided for the remainder driver circuitry [*Figs. 1(A): outputting at q_{n-1} and q_n*].

In such a manner, ***Takeda*** reads on the general driver horizontal shift register circuit and the remainder driver horizontal shift register circuit of the instantly claimed invention.

However, should it be shown that ***Takeda*** neglects teaching the "*general and remainder driver horizontal shift register circuitry*" subject matter with sufficient specificity:

Hirai discloses a liquid crystal display [*Fig. 1*] comprising:

a display portion [*Fig. 1: LCD 26*], said display portion having

a plurality of gate lines,

a plurality of signal lines [*Fig. 1: Y*] and

a plurality of pixels,

a pixel of said plurality of pixels being located at an intersection of a gate line of said plurality of gate lines and a signal line of said plurality of signal lines; and

a plurality of driver circuits [*Fig. 1: 18 and Figs. 3-5: 20*], said plurality of driver circuits including

at least one general driver circuit [*Fig. 5: each of the first two leftmost driving integrated circuits 20 constituting one general driver circuit*] and

one remainder driver circuit [*Fig. 5: the last, rightmost driving integrated circuit 20*],

each said at least one general driver circuit having

a general driver horizontal shift register circuit [*Figs. 1 & 2: shift register 11 and Fig. 3: bidirectional shift register 21*] and

a plurality of general driver circuit output terminals [*Fig. 5:* Y_1-Y_{80}],

a general driver circuit output terminal of said plurality of general driver circuit output terminals providing a signal potential to one of said plurality of signal lines (*Column 4, Line 15 - Column 5, Line 42*),

said remainder driver circuit having a remainder driver horizontal shift register circuit [*Figs. 1 & 2: shift register 11 and Fig. 3: bidirectional shift register 21*] and

a plurality of remainder driver circuit output terminals [*Fig. 5:* Y_1-Y_{16}],

a remainder driver circuit output terminal of said plurality of remainder driver circuit output terminals providing another signal potential to another of said plurality of signal lines,

the quantity [*16*] of said remainder driver circuit output terminals [*Fig. 5:* Y_1-Y_{16}] being defined as (S - (OP * (DC-1))),

"S" being the quantity [*176*] of said plurality of signal lines [*Fig. 5:* $(Y_1$-$Y_{80})$ + $(Y_1$-$Y_{80})$ + $(Y_1$-$Y_{16})$ = Y_{176}],

"OP" being the quantity [*80*] of said general driver circuit output terminals [*Fig. 5:* Y_1-Y_{80}], and

"DC" being the quantity [*3*] of said plurality of driver circuits [*Fig. 5: two leftmost general driver circuits and one rightmost remainder driver circuit = three driver circuits total*] , and

said quantity [*80*] of said general driver circuit output terminals being different than said quantity [*16*] of said remainder driver circuit output terminals (*Column 1, Line 5 - Column 2, Line 60*).

Hirai also discloses the shift register circuit [*Fig. 2, 11*] is being comprised by a series of distinct flip flops [*Fig. 2,* FF_1-FF_{80}] set up in a linear fashion which have their inputs and outputs connected together in such a way that the data [*Fig. 2, DI*] are shifted down the line [*Fig. 2,* Y_1-Y_{80}] when the circuit is activated [*Fig. 2, via clock signal CL2*] (*Column 4, Line 22 - Column 5, Line 42*).

Should it be shown that ***Hirai*** neglects teaching a pixel of said plurality of pixels being located at an intersection of a gate line of said plurality of gate lines and a signal line of said plurality of signal lines with sufficient specificity; the examiner takes official notice that it would have been obvious to an artisan to incorporate such an active matrix type structure, so as to provide a light weight display having very good image quality, wide color gamut, and relatively fast response time. Moreover, as already detailed above, ***Takeda*** teaches such subject matter.

Takeda and ***Hirai*** are analogous art, because they are from the shared inventive field of using shift register circuitry to drive a liquid crystal display.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use ***Hirai's*** integrated shift register circuitry to drive ***Takeda's*** liquid crystal display device, so as to use a conventional type of shift register and to eliminate the need for mixing serial data to be input with dummy data even if the necessary total of output bits cannot be divided by the number of output bits of a single IC.

Moreover, it would have been obvious to an artisan to combine ***Hirai's*** 80-pin output drivers [*Fig. 5:* Y_1-Y_{80}] with ***Takeda's*** N-pin output drivers [*Fig. 1(A):* Q_1-Q_N], so as to provide a

total number of output pins equaling the total number of display signal lines -- resulting in the instantly claimed invention in every incarnation where ***Takeda's*** N does not also equal 80.

It would have been obvious to one of ordinary skill in the art at the time of invention because all the claimed elements were known in the prior art and one skilled in the art could have combined the integrated shift register and driver circuitry as claimed by known methods with no change in their respective functions, and the combination would have yielded predictable results to one of ordinary skill in the art at the time of the invention.

Regarding claim 26, ***Takeda*** discloses one driver circuit of said plurality of driver circuits is separate and distinct from another driver circuit of said plurality of driver circuits [*Fig. 1(A)*].

Hirai discloses one driver circuit of said plurality of driver circuits is separate and distinct from another driver circuit of said plurality of driver circuits (*Column 4, Line 22 - Column 5, Line 42*).

Regarding claim 27, ***Takeda*** discloses said plurality of pixels is arranged in a two-dimensional matrix shape (*Fig. 2*).

Hirai discloses said plurality of pixels is arranged in a two-dimensional matrix shape (*Fig. 3*).

Regarding claim 28, ***Takeda*** discloses said pixel of said plurality of pixels includes a transistor [*Fig. 2, 11-d*], a gate electrode [*Fig. 2, at 11-a*] of said transistor being electrically

connected to said gate line, a source/drain [*Fig. 2, at 11-b*] of said transistor being electrically connected to said signal line (*Fig. 2; Column 2, Lines 56-68*).

Hirai discloses said pixel of said plurality of pixels includes a transistor, a gate electrode of said transistor being electrically connected to said gate line, a source/drain of said transistor being electrically connected to said signal line (*Column 4, Line 22 - Column 5, Line 42*).

Regarding claim 29, ***Takeda*** discloses said plurality of gate lines is a plurality of rows and said plurality of signal lines is a plurality of columns (*Fig. 2*).

Hirai discloses said plurality of gate lines is a plurality of rows and said plurality of signal lines is a plurality of columns (*Column 4, Line 22 - Column 5, Line 42*).

Regarding claim 31, ***Takeda*** discloses a surplus connecting region [*Fig. 2; 12, 13, & 15*] that does not contribute to said display portion [*Fig. 2, 11*] does not occur on the said display (*Column 2, Line 56 - Column 3, Line 27*).

Hirai discloses a surplus connecting region that does not contribute to said display portion does not occur on the said display (*Fig. 5; Column 1, Line 5 - Column 2, Line 60*).

Regarding claim 37, ***Takeda*** discloses an output terminal of said plurality of driver circuits is electrically connected to an input terminal of a time-divisional switch [*Fig. 1(A), 32*], said time-divisional switch providing a de-multiplexed signal potential to said signal line, said de-multiplexed signal potential being a signal potential for one of a plurality of primary colors

that is time-divided from another signal potential for another of said plurality of primary colors and supplied to said signal line (*Column 4, Lines 22-68*).

Hirai discloses an output terminal of said plurality of driver circuits is electrically connected to an input terminal of a time-divisional switch, said time-divisional switch providing a de-multiplexed signal potential to said signal line, said de-multiplexed signal potential being a signal potential for one of a plurality of primary colors that is time-divided from another signal potential for another of said plurality of primary colors and supplied to said signal line (*Fig. 3; Column 1, Line 5 - Column 2, Line 60*).

Regarding claim 43, ***Takeda*** discloses said plurality of primary colors is a first primary color, a second primary color and a third primary color (*Column 2, Lines 55-68*).

Hirai discloses said plurality of primary colors is a first primary color, a second primary color and a third primary color (*Column 4, Line 22 - Column 5, Line 42*).

Regarding claim 44, ***Takeda*** discloses said quantity [*3*] of general driver circuit output terminals is greater than said quantity [*2*] of remainder driver circuit output terminals [*Fig. 1(A)*].

Hirai discloses said quantity of general driver circuit output terminals is greater than said quantity of remainder driver circuit output terminals (*Fig. 5; Column 1, Line 5 - Column 2, Line 60*).

Regarding claim 45, ***Takeda*** discloses the sum total of general driver circuit output terminals [*3*] and said remainder driver circuit output terminals [*2*] is equal to said plurality of signal lines [*5*] [*Fig. 1(A)*].

Hirai discloses the sum total of general driver circuit output terminals and said remainder driver circuit output terminals is equal to said plurality of signal lines (*Fig. 5; Column 1, Line 5 - Column 2, Line 60*).

Regarding claim 46, ***Takeda*** discloses said plurality of driver circuits includes more than one said general driver circuit [*Fig. 1(A)*].

Hirai discloses said plurality of driver circuits includes more than one said general driver circuit (*Fig. 5; Column 1, Line 5 - Column 2, Line 60*).

Regarding claim 47, ***Takeda*** discloses said each said general driver circuit has an equal number of general driver circuit output terminals [*Fig. 1(A)*].

Hirai discloses said each said general driver circuit has an equal number of general driver circuit output terminals (*Fig. 5; Column 1, Line 5 - Column 2, Line 60*).

Regarding claim 48, ***Takeda*** discloses said plurality of driver circuits are driver integrated circuits arranged in an outside of a transparent insulating substrate on which said display portion is formed (*Fig. 2; Column 2, Line 56 - Column 4, Line 6*).

Takeda states, "*FIG. 2 is a block diagram which explains a general configuration of the liquid crystal color display device used in this invention. Numeral (11) in the figure is the liquid*

crystal color display panel. Switching transistors 11-d are built into the display picture elements 11-c, which are the intersecting points of the row electrodes 11-a and column electrodes 11-b on one of the circuit boards of the panel (11). On the other circuit board, there are counter electrodes, and respective color filters: red (R), green (G) and blue (B) opposing the display picture elements, arranged, for example, as shown in the diagram" (Column 2, Lines 56-68).

As such at least one of ***Takeda's*** circuit boards would necessarily, inherently, and obviously be both "*transparent*" and "*insulating*." If neither of the circuit boards was transparent, it would not be possible to see ***Takeda's*** pixels, thereby preventing ***Takeda's*** invention from being "*a display*."

Moreover, circuit boards are by, definition, "*insulating*." For example: Random House Dictionary defines "*circuit board*" as "*a sheet of insulating material used for the mounting and interconnection (often by a printed circuit) of components in electronic equipment*."

Additionally, ***Takeda's*** disclosed color filters and twisted nematic liquid crystal layer would both constitute "*a transparent insulating substrate*," as instantly claimed.

Hirai also discloses said plurality of driver circuits are driver integrated circuits arranged in an outside of a transparent insulating substrate on which said display portion is formed (*Fig. 5; Column 1, Line 5 - Column 2, Line 60*).

Here too, ***Hirai's*** disclosed liquid crystal layer would both constitute "*a transparent insulating substrate*," as instantly claimed.

Finally, it would have been obvious to one having ordinary skill in the art at the time of invention to form a display portion on a transparent insulating substrate (*such as glass*), as is customary and conventional in the field of liquid crystal displays (*as is acknowledged in on the very first page of the instant application's specification -- see page 1, line 20*).

Regarding claim 71, ***Hirai*** discloses one general driver horizontal shift register circuit of said plurality of driver circuits is separate and distinct from another general driver horizontal shift register circuit of said plurality of driver circuits (*Figs. 3 & 5; Column 1, Line 5 - Column 2, Line 60*).

Takeda discloses one general driver horizontal shift register circuit of said plurality of driver circuits is separate and distinct from another general driver horizontal shift register circuit of said plurality of driver circuits (*Fig. 2; Column 2, Line 56 - Column 4, Line 6*).

Regarding claim 72, ***Hirai*** discloses said general driver horizontal shift register circuit performs a horizontal scan by sequentially generating horizontal scanning pulses (*Figs. 1 & 2; Column 4, Line 22 - Column 5, Line 42*).

Takeda discloses said general driver horizontal shift register circuit performs a horizontal scan by sequentially generating horizontal scanning pulses (*Fig. 2; Column 2, Line 56 - Column 4, Line 6*).

Regarding claim 73, ***Hirai*** discloses said each said at least one general driver circuit has general driver sampling switches [*Fig. 2, FF1-FF80*], a general driver level shifter [*Fig. 1, 23*], a

general driver data latch circuit [*Fig. 1, 22*], and a general driver digital/analog converting circuit [*Fig. 1, 22*] (*Column 4, Line 22 - Column 5, Line 42*).

Takeda discloses said each said at least one general driver circuit has general driver sampling switches, a general driver level shifter, a general driver data latch circuit, and a general driver digital/analog converting circuit (*Fig. 2; Column 2, Line 56 - Column 4, Line 6*).

Should it be shown that ***Hirai*** neglects teaching a digital/analog converting circuit with sufficient specificity; the examiner takes official notice that it would have been obvious to an artisan to incorporate digital/analog converting circuitry, so as to assure that all signals are at appropriate levels.

Regarding claim 74, ***Hirai*** discloses sampling switches [*Fig. 2, FF1-FF80*] in said general driver sampling switches sequentially sample input digital image data in response to horizontal scanning pulses from said general driver horizontal shift register circuit (*Column 4, Line 22 - Column 5, Line 42*).

Takeda discloses sampling switches in said general driver sampling switches sequentially sample input digital image data in response to horizontal scanning pulses from said general driver horizontal shift register circuit (*Fig. 2; Column 2, Line 56 - Column 4, Line 6*).

Should it be shown that ***Hirai*** neglects teaching a digital data with sufficient specificity; the examiner takes official notice that it would have been obvious to an artisan to use digital signals, so as to assure that all signals are at appropriate levels.

Regarding claim 75, ***Hirai*** discloses said general driver level shifter boosts digital data sampled by said general driver sampling switches to digital data of a liquid crystal driving voltage (*Column 4, Line 22 - Column 5, Line 42*).

Takeda discloses said general driver level shifter boosts digital data sampled by said general driver sampling switches to digital data of a liquid crystal driving voltage (*Fig. 2; Column 2, Line 56 - Column 4, Line 6*).

Should it be shown that ***Hirai*** neglects teaching a digital data with sufficient specificity; the examiner takes official notice that it would have been obvious to an artisan to use digital signals, so as to assure that all signals are at appropriate levels.

Regarding claim 76, ***Hirai*** discloses said general driver data latch circuit is a memory to accumulate digital data boosted by said general driver level shifter by an amount of one horizontal period (*Column 4, Line 22 - Column 5, Line 42*).

Takeda discloses said general driver data latch circuit is a memory to accumulate digital data boosted by said general driver level shifter by an amount of one horizontal period (*Fig. 2; Column 2, Line 56 - Column 4, Line 6*).

Should it be shown that ***Hirai*** neglects teaching a digital data with sufficient specificity; the examiner takes official notice that it would have been obvious to an artisan to use digital signals, so as to assure that all signals are at appropriate levels.

Regarding claim 77, ***Hirai*** discloses said general driver digital/analog converting circuit converts digital data of one horizontal period which is outputted from said general driver data

latch circuit into an analog signal and outputs said analog signal (*Column 4, Line 22 - Column 5, Line 42*).

Takeda discloses said general driver digital/analog converting circuit converts digital data of one horizontal period which is outputted from said general driver data latch circuit into an analog signal and outputs said analog signal (*Fig. 2; Column 2, Line 56 - Column 4, Line 6*).

Should it be shown that ***Hirai*** neglects teaching a digital/analog converting circuit with sufficient specificity; the examiner takes official notice that it would have been obvious to an artisan to incorporate digital/analog converting circuitry, so as to assure that all signals are at appropriate levels.

Regarding claim 78, ***Hirai*** discloses said remainder driver circuit has remainder driver sampling switches [*Fig. 2, FF1-FF80*], a remainder driver level shifter [*Fig. 1, 23*], a remainder driver data latch circuit [*Fig. 1, 22*], and a remainder driver digital/analog converting circuit [*Fig. 1, 22*] (*Column 4, Line 22 - Column 5, Line 42*).

Takeda discloses said remainder driver circuit has remainder driver sampling switches, a remainder driver level shifter, a remainder driver data latch circuit, and a remainder driver digital/analog converting circuit (*Fig. 2; Column 2, Line 56 - Column 4, Line 6*).

Should it be shown that ***Hirai*** neglects teaching a digital/analog converting circuit with sufficient specificity; the examiner takes official notice that it would have been obvious to an artisan to incorporate digital/analog converting circuitry, so as to assure that all signals are at appropriate levels.

Claim Rejections - 35 USC § 103

4. Claims 49-66 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Takeda et al (US 4,825,203 A)*** in view of ***Lee (US 5,426,447 A)***.

Regarding claim 49, ***Takeda*** discloses a liquid crystal display [*Fig. 2*] comprising:

a display portion [*Fig. 2: liquid crystal color display panel 11*], said display portion having

a plurality of gate lines [*Fig. 2: row electrodes 11-a*],

a plurality of signal lines [*Fig. 2: column electrodes 11-b*] and

a plurality of pixels [*Fig. 2: RGB display picture elements 11-c*],

a pixel of said plurality of pixels being located at an intersection of a gate line of said plurality of gate lines and a signal line of said plurality of signal lines (*see Fig. 2*); and

a plurality of driver circuits (*wherein the total column electrode drive circuit [Fig. 2: 13] is made up by a plurality of single column driver circuits, each single column driver circuit comprising:*

a shift register [Fig. 1(A): 31],

an output terminal [Fig. 1(A): q],

three AND gate circuits [Fig. 1(A): 37],

three analog switches [Fig. 1(A): 32],

a first condenser [Fig. 1(A): 33],

another analog switch [Fig. 1(A): 34],

a second condenser [Fig. 1(A): 35],

an output buffer [Fig. 1(A): 36], and

a column electrode output terminal [Fig. 1(A): Q]) (*see Column 2, Line 56 - Column 3, Line 27*),

each of said plurality of driver circuits having a plurality of driver circuit output terminals (*e.g., an arbitrary pairing of every two adjacent column driver circuits [Fig. 1(A): ($q_{1\text{-}2}$ to $Q_{1\text{-}2}$), ($q_{3\text{-}4}$ to $Q_{3\text{-}4}$), ... , ($q_{N\text{-}1,\,N}$ to $Q_{N\text{-}1,\,N}$)]*),

a driver circuit output terminal [*Fig. 1(A): output terminals $Q_{1\text{-}2}$ from output buffers $36_{1\text{-}2}$; output terminals $Q_{3\text{-}4}$ from output buffers $36_{3\text{-}4}$; ... ; and output terminals $Q_{N\text{-}1,\,N}$ from output buffers $36_{N\text{-}1,\,N}$*] of said a plurality of driver circuit output terminals providing a signal potential ("*a signal corresponding to the display pattern*") to a signal line of said plurality of signal lines (*wherein output terminals [Fig. 1(A): $Q_{1\text{-}N}$] from output buffers [Fig. 1(A): $36_{1\text{-}N}$] output display signals to the corresponding column electrode lines [Fig. 2: column electrodes 11-b])*,

the quantity [*2*] of said driver circuit output terminals [*Fig. 1(A): two output terminals for each of: $Q_{1\text{-}2}$; $Q_{3\text{-}4}$; $Q_{N\text{-}1,\,N}$*] being the same quantity for said each of said plurality of driver circuits, and

the quantity of said driver circuits being defined as N/n [*$N / n = 6 / 2 = 3$ driver circuits : first driver circuit ($q_{1\text{-}2}$ to $Q_{1\text{-}2}$), second driver circuit ($q_{3\text{-}4}$ to $Q_{3\text{-}4}$), and third driver circuit ($q_{5\text{-}6}$ to $Q_{5\text{-}6}$)*], wherein

"N" is the quantity [*Fig. 1(A): e.g., for simplicity's sake arbitrarily set N = 6 column signal lines. However please note, the number of column signal lines could be set as high as desired. Simply increase the number of driver circuits accordingly and the instantly claimed equation will still work.*] of said signal lines and

"n" is said quantity [*2*] of said driver circuit output terminals [*Fig. 1(A): two output terminals for each of:* Q_{1-2}; Q_{3-4}; $Q_{N-1, N}$] (*Column 4, Lines 22-68*).

Claim 49 is claiming little more than a display having two driver circuits (*both driver circuits having the same number of outputs*).

It is the examiner's contention that such a broad claim would read on most any display having four or more line drivers -- which can be arbitrarily combined into two driver circuit pairs/groups (*with each driver circuit pair/group having the same number of outputs*).

Takeda does not expressly use the explicit term, "*pixel*" when describing the structure of the liquid crystal display.

Should it be shown that ***Takeda*** neglects teaching the "*pixel*" subject matter with sufficient specificity:

Lee discloses a transparent insulating substrate (*e.g. glass*) on which a display portion comprising a plurality of "*pixels*" is formed (*Column 1, Lines 18-30*).

Takeda and ***Lee*** are analogous art, because they are from the shared field of liquid crystal display device structures.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use ***Lee's*** "*pixel*" terminology to describe ***Takeda's*** "*display picture elements*", so as to make use of common terminology in the art.

Regarding claim 50, ***Takeda*** discloses a plurality of time-divisional switches [*Fig. 1(A), 32*], said plurality of time-divisional switches receiving said signal potential from said driver circuit output terminal and time-divisionally sending said received signal potential said signal line (*Column 4, Lines 22-68*).

Regarding claim 51, ***Takeda*** discloses the quantity of said time-divisional switches is equal to 3 [*Fig. 1(A), 32*] (*Column 4, Lines 22-68*).

Regarding claim 52, ***Takeda*** discloses said quantity of said signal lines is different than said quantity of said driver circuit output terminals (*Fig. 1(A) and Column 4, Lines 22-68*).

Regarding claim 53, ***Takeda*** discloses said quantity of said driver circuit output terminals is set to a power of 2 (*Fig. 1(A) and Column 4, Lines 22-68*).

Regarding claim 54, although ***Takeda's*** *Figures 1(A) and 2* render it readily apparent that the column electrode drive circuit [*13*] comprises driver ICs outside the display substrate [*11*], and although every material presently known to man possesses an inherent insulative capacity, and although it's arguable that the ***Takeda's*** LCD must feature at least one transparent substrate in order for a user to actually view a displayed image, ***Takeda*** does not expressly use the explicit term, "*transparent insulating substrate*" when describing the structure of the liquid crystal display.

However, ***Lee*** does disclose a transparent insulating substrate (*e.g. glass*) on which a display portion is formed (*Column 1, Lines 28-30*).

Takeda and ***Lee*** are analogous art, because they are from the shared field of liquid crystal display device structures.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use ***Lee's*** transparent insulating glass substrate to form ***Takeda's*** liquid crystal display, so as to make it possible for users to actually view any displayed images.

Regarding claim 55, ***Takeda*** discloses a memory circuit [*Fig. 1(A), 31*] for temporarily storing data [*Fig. 1(A), D*] to be written into said plurality of driver circuits; and a control circuit [*Fig. 2, 15*] for controlling said plurality of driver circuits so as to simultaneously write different data from said memory circuit (*Column 3, Lines 8-27 & Column 4, Lines 22-68*).

Regarding claim 56, ***Takeda*** discloses a leading waveform and a trailing waveform of a signal output waveform [*Fig. 1(B),* C_R, C_G & C_B] of each of said plurality of driver circuits are symmetrical with respect to a time base (*Column 4, Lines 47-68*).

Regarding claim 57, ***Takeda*** discloses a period of time which is selected by said time-divisional switches is equal to or shorter than 1/3 of a horizontal scanning period (*Fig. 1(B); Column 4, Line 22 - Column 5, Line 15*).

Regarding claim 58, ***Takeda*** discloses a leading time and a trailing time of each of said plurality of driver circuits are equal to or shorter than the period of time which is selected by said time-divisional switches (*Fig. 1(B); Column 4, Line 22 - Column 5, Line 15*).

Regarding claim 59, ***Takeda*** discloses a blanking period which is caused for the period of time, selected by said time-divisional switches is equal to or shorter than (a horizontal Scanning period - the period of time selected by the time-divisional switches x 3) / 3 (*Fig. 1(B); Column 4, Line 22 - Column 5, Line 15*).

Regarding claim 60, ***Takeda*** discloses said plurality of driver circuits have a function to stop the operation of an output circuit of said plurality of driver circuits for said blanking period (*Fig. 1(B); Column 4, Line 22 - Column 5, Line 15*).

Regarding claim 61, ***Takeda*** discloses said plurality of driver circuits generate a signal potential so as to correct curves of voltage-transmittance characteristics of R (red), G (green), and G (blue) [*Fig. 1(A),* V_R, V_G & V_B] by diving to said time-divisional switches (*Column 4, Lines 22-46*).

Regarding claim 62, ***Takeda*** discloses within a 1H (H denotes a horizontal scanning period) inversion driving or a 1H common inversion driving, the signal line which is selected first by said time-divisional switches is a line of blue, the signal line which is selected at the

second time is a line of green, and the signal line which is selected at the third time is a line of red [*Fig. 4(B); Row i+2 & Columns j, j+1 and j+2*].

Regarding claim 63, ***Takeda*** discloses within a dot inversion driving, the signal line which is selected first by said time-divisional switches is a line of red, the signal line which is selected at the second time is a line of green, and the signal line which is selected at the third time is a line of blue [*Fig. 5(B); Row i & Columns j, j+1 and j+2*].

Regarding claim 64, ***Takeda*** discloses time-division of said time- division switches distribute signals to R (red), G (green), and G (blue) constituting one pixel [*Figs. 4(A-B); Column 5, Lines 16-58*].

Regarding claim 65, ***Takeda*** discloses a surplus connecting region [*Fig. 2; 12, 13, & 15*] that does not contribute to said display portion [*Fig. 2, 11*] does not occur on the said display (*Column 2, Line 56 - Column 3, Line 27*).

Regarding claim 66, ***Takeda*** discloses said driver circuits is separate and distinct from another driver circuit of said plurality of driver circuits [*Fig. 1(A)*].

Claim Rejections - 35 USC § 103

5. Claims 67-70 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Takeda et al (US 4,825,203 A)*** and ***Lee (US 5,426,447 A)*** as applied to *claim 49* above, and further in view of ***Hirai (US 5,440,304 A)***.

Regarding claim 67, ***Takeda*** discloses said each of said plurality of driver circuits has a horizontal shift register circuit [*Fig. 1(a); 31*] (*Column 4, Lines 22-68*).

Lee discloses said each of said plurality of driver circuits has a horizontal shift register circuit [*Fig. 1; 49*] (*Column 4, Line 47 - Column 5, Line 39*).

Should it be shown that neither ***Takeda*** nor ***Lee*** teaches a horizontal shift register circuit with sufficient specificity:

Hirai discloses a liquid crystal display [*Fig. 4*] comprising:

a display portion [*Fig. 4: LCD 26*], said display portion having

a plurality of gate lines,

a plurality of signal lines [*Fig. 4: Y*], and

a plurality of pixels,

a pixel of said plurality of pixels being located at an intersection of a gate line of said plurality of gate lines and a signal line of said plurality of signal lines; and

a plurality of driver circuits [*Fig. 4: 20*],

each of said plurality of driver circuits [*Fig. 5: first driver circuit Y_1-Y_{72}; second driver circuit Y_{73}-Y_{144}; and third driver circuit Y_{145}-Y_{216}*] having a plurality of driver circuit output terminals [*Fig. 4: Y_1-Y_{72}*],

a driver circuit output terminal of said a plurality of driver circuit output terminals providing a signal potential to a signal line of said plurality of signal lines,

the quantity [*Fig. 4: 72*] of said driver circuit output terminals [*Fig. 4: Y_1-Y_{72}*] being the same quantity for said each of said plurality of driver circuits (*see Fig. 4*), and

the quantity of said driver circuits being defined as N/n [*N / n = 216 / 72 = 3 driver circuits: first driver circuit Y_1-Y_{72}; second driver circuit Y_{73}-Y_{144}; and third driver circuit Y_{145}-Y_{216}*] , wherein

"N" is the quantity of said signal lines [*N = 72 + 72 +72 = 216*] and

"n" is said quantity [*n= 72*] of said driver circuit output terminals [*Fig. 4: Y_1-Y_{72}*];

wherein

said each of said plurality of driver circuits has a horizontal shift register circuit [*Figs. 1 & 2; 11 and Fig. 3; 21*] (*Column 4, Line 15 - Column 5, Line 42*).

Takeda, ***Lee***, and ***Hirai*** are analogous art, because they are from the shared inventive field of using shift register circuitry to drive liquid crystal displays.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use ***Hirai's*** integrated shift register circuitry to drive ***Lee*** and ***Takeda's*** combined liquid crystal display device, so as to use a conventional type of shift register and to eliminate the

need for mixing serial data to be input with dummy data even if the necessary total of output bits cannot be divided by the number of output bits of a single IC.

Moreover, it would have been obvious to an artisan to combine ***Hirai's*** 80-pin output drivers [*Fig. 5:* Y_1-Y_{80}], or alternately ***Hirai's*** 72-pin output drivers [*Fig. 4:* Y_1-Y_{72}], with ***Takeda's*** N-pin output drivers [*Fig. 1(A):* Q_1-Q_N], so as to provide a total number of output pins equaling the total number of display signal lines -- resulting in the instantly claimed invention in every incarnation where ***Takeda's*** *N* also equals 80, or alternately 72.

Regarding claim 68, ***Hirai*** discloses one general driver horizontal shift register circuit of said plurality of driver circuits is separate and distinct from another general driver horizontal shift register circuit of said plurality of driver circuits (*Figs. 3 & 5; Column 1, Line 5 - Column 2, Line 60*).

Regarding claim 69, ***Hirai*** discloses said horizontal shift register circuit performs a horizontal scan by sequentially generating horizontal scanning pulses (*Figs. 1 & 2; Column 4, Line 22 - Column 5, Line 42*).

Regarding claim 70, ***Hirai*** discloses said horizontal shift register circuit has sampling switches [*Fig. 2, FF1-FF80*], a level shifter [*Fig. 1, 23*], a data latch circuit [*Fig. 1, 22*], and a digital/analog converting circuit [*Fig. 1, 22*] (*Column 4, Line 22 - Column 5, Line 42*).

Should it be shown that ***Hirai*** neglects teaching a digital/analog converting circuit with sufficient specificity; the examiner takes official notice that it would have been obvious to an

artisan to incorporate digital/analog converting circuitry, so as to assure that all signals are at appropriate levels.

Claim Rejections - 35 USC § 102

6. Claim 49 is rejected under 35 U.S.C. 102(b) as being anticipated by ***Hayashi et al (US 4,745,406 A)***.

Regarding claim 49, ***Hayashi*** discloses a liquid crystal display [*Fig. 8*] comprising:

a display portion [*Fig. 8: P*], said display portion having

a plurality of gate lines [*Fig. 8: G*],

a plurality of signal lines [*Fig. 8: Columns 1-4 driven by transistors* M_{1-4}] and

a plurality of pixels [*Fig. 8: Pst*],

a pixel of said plurality of pixels being located at an intersection of a gate line of said plurality of gate lines and a signal line of said plurality of signal lines; and

a plurality of driver circuits [*Fig. 8: "the first driver circuit" =* (M_1 *and* M_2) *and "the second driver circuit" =* (M_3 *and* M_4)],

each of said plurality of driver circuits having a plurality of driver circuit output terminals [*Fig. 8: "the first driver circuit" =* (M_1 *and* M_2) *has two output terminals driving the first two column electrodes and "the second driver circuit" =* (M_3 *and* M_4) *has two output terminals driving the second two column electrodes*],

a driver circuit output terminal of said a plurality of driver circuit output terminals providing a signal potential to a signal line of said plurality of signal lines,

the quantity [*2*] of said driver circuit output terminals being the same quantity for said each of said plurality of driver circuits [*Fig. 8: "the first driver circuit" = (M_1 and M_2) has two output terminals driving the first two column electrodes and "the second driver circuit" = (M_3 and M_4) has two output terminals driving the second two column electrodes*], and

the quantity of said driver circuits being defined as N/n [*N / n = 4 / 2 = 2 driver circuits: Fig. 8: "the first driver circuit" = (M_1 and M_2) and "the second driver circuit" = (M_3 and M_4)*] , wherein

"N" is the quantity [*4*] of said signal lines [*Fig. 8: Columns 1-4*] and

"n" is said quantity [*2*] of said driver circuit output terminals [*Fig. 8: "the first driver circuit" = (M_1 and M_2) has two output terminals driving the first two column electrodes and "the second driver circuit" = (M_3 and M_4) has two output terminals driving the second two column electrodes*] (*Column 4, Line 43 - Column 5, Line 8*).

Claim Rejections - 35 USC § 103

7. Claims 67-70 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Hayashi et al (US 4,745,406 A)*** in view of ***Hirai (US 5,440,304 A)***.

Regarding claim 67, ***Hayashi*** discloses said each of said plurality of driver circuits has a horizontal shift register circuit [*Fig. 8; 2*] (*Column 4, Line 43 - Column 5, Line 8*).

Should it be shown that ***Hayashi*** neglects teaching a horizontal shift register circuit with sufficient specificity:

Hirai discloses a liquid crystal display [*Fig. 4*] comprising:

a display portion [*Fig. 4: LCD 26*], said display portion having

a plurality of gate lines,

a plurality of signal lines [*Fig. 4: Y*], and

a plurality of pixels,

a pixel of said plurality of pixels being located at an intersection of a gate line of said plurality of gate lines and a signal line of said plurality of signal lines; and

a plurality of driver circuits [*Fig. 4: 20*],

each of said plurality of driver circuits [*Fig. 5: first driver circuit Y_1-Y_{72}; second driver circuit Y_{73}-Y_{144}; and third driver circuit Y_{145}-Y_{216}*] having a plurality of driver circuit output terminals [*Fig. 4: Y_1-Y_{72}*],

a driver circuit output terminal of said a plurality of driver circuit output terminals providing a signal potential to a signal line of said plurality of signal lines,

the quantity [*Fig. 4: 72*] of said driver circuit output terminals [*Fig. 4: Y_1-Y_{72}*] being the same quantity for said each of said plurality of driver circuits (*see Fig. 4*), and

the quantity of said driver circuits being defined as N/n [*N / n = 216 / 72 = 3 driver circuits: first driver circuit Y_1-Y_{72}; second driver circuit Y_{73}-Y_{144}; and third driver circuit Y_{145}-Y_{216}*] , wherein

"N" is the quantity of said signal lines [*N = 72 + 72 +72 = 216*] and

"n" is said quantity [*n= 72*] of said driver circuit output terminals [*Fig. 4: Y_1-Y_{72}*];

wherein

said each of said plurality of driver circuits has a horizontal shift register circuit [*Figs. 1 & 2; 11 and Fig. 3; 21*] (*Column 4, Line 15 - Column 5, Line 42*).

Hayashi and ***Hirai*** are analogous art, because they are from the shared inventive field of using shift register circuitry to drive liquid crystal displays.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use ***Hirai's*** integrated shift register circuitry to drive ***Hayashi's*** liquid crystal display device, so as to use a conventional type of shift register and to eliminate the need for mixing serial data to be input with dummy data even if the necessary total of output bits cannot be divided by the number of output bits of a single IC.

Moreover, it would have been obvious to an artisan to combine ***Hirai's*** 80-pin output drivers [*Fig. 5:* Y_1-Y_{80}], or alternately ***Hirai's*** 72-pin output drivers [*Fig. 4:* Y_1-Y_{72}], with ***Hayashi's*** M_{s+N} pin shift register circuitry [*Fig. 8: 2*], so as to provide a total number of output pins equaling the total number of display signal lines -- resulting in the instantly claimed invention in every incarnation where ***Hayashi's*** *N* also equals 79, or alternately 71.

Regarding claim 68, ***Hirai*** discloses one general driver horizontal shift register circuit of said plurality of driver circuits is separate and distinct from another general driver horizontal shift register circuit of said plurality of driver circuits (*Figs. 3 & 5; Column 1, Line 5 - Column 2, Line 60*).

Regarding claim 69, ***Hirai*** discloses said horizontal shift register circuit performs a horizontal scan by sequentially generating horizontal scanning pulses (*Figs. 1 & 2; Column 4, Line 22 - Column 5, Line 42*).

Regarding claim 70, ***Hirai*** discloses said horizontal shift register circuit has sampling switches [*Fig. 2, FF1-FF80*], a level shifter [*Fig. 1, 23*], a data latch circuit [*Fig. 1, 22*], and a digital/analog converting circuit [*Fig. 1, 22*] (*Column 4, Line 22 - Column 5, Line 42*).

Should it be shown that ***Hirai*** neglects teaching a digital/analog converting circuit with sufficient specificity; the examiner takes official notice that it would have been obvious to an artisan to incorporate digital/analog converting circuitry, so as to assure that all signals are at appropriate levels.

Claim Rejections - 35 USC § 102 / 103

8. Claims 67-70 are rejected under 35 U.S.C. 102(b) as anticipated by ***Hirai (US 5,440,304 A)***.

9. Or, in the alternative, claims 67-70 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Hirai (US 5,440,304 A)***.

Regarding claim 67, ***Hirai*** discloses a liquid crystal display [*Fig. 4*] comprising:

a display portion [*Fig. 4: LCD 26*], said display portion having

a plurality of gate lines,

a plurality of signal lines [*Fig. 4: Y*], and

a plurality of pixels,

a pixel of said plurality of pixels being located at an intersection of a gate line of said plurality of gate lines and a signal line of said plurality of signal lines; and

a plurality of driver circuits [*Fig. 4: 20*],

each of said plurality of driver circuits [*Fig. 5: first driver circuit Y_1-Y_{72}; second driver circuit Y_{73}-Y_{144}; and third driver circuit Y_{145}-Y_{216}*] having a plurality of driver circuit output terminals [*Fig. 4: Y_1-Y_{72}*],

a driver circuit output terminal of said a plurality of driver circuit output terminals providing a signal potential to a signal line of said plurality of signal lines,

the quantity [*Fig. 4: 72*] of said driver circuit output terminals [*Fig. 4: Y_1-Y_{72}*] being the same quantity for said each of said plurality of driver circuits (*see Fig. 4*), and

the quantity of said driver circuits being defined as N/n [*N / n = 216 / 72 = 3 driver circuits: first driver circuit Y_1-Y_{72}; second driver circuit Y_{73}-Y_{144}; and third driver circuit Y_{145}-Y_{216}*] , wherein

"N" is the quantity of said signal lines [*N = 72 + 72 +72 = 216*] and

"n" is said quantity [*n= 72*] of said driver circuit output terminals [*Fig. 4: Y_1-Y_{72}*];

wherein

said each of said plurality of driver circuits has a horizontal shift register circuit [*Figs. 1 & 2; 11 and Fig. 3; 21*] (*Column 4, Line 15 - Column 5, Line 42*).

Should it be shown that ***Hirai*** neglects teaching a pixel of said plurality of pixels being located at an intersection of a gate line of said plurality of gate lines and a signal line of said

plurality of signal lines with sufficient specificity; the examiner takes official notice that it would have been obvious to an artisan to incorporate such an active matrix type structure, so as to provide a light weight display having very good image quality, wide color gamut, and relatively fast response time.

Regarding claim 68, ***Hirai*** discloses one general driver horizontal shift register circuit of said plurality of driver circuits is separate and distinct from another general driver horizontal shift register circuit of said plurality of driver circuits (*Figs. 3 & 5; Column 1, Line 5 - Column 2, Line 60*).

Regarding claim 69, ***Hirai*** discloses said horizontal shift register circuit performs a horizontal scan by sequentially generating horizontal scanning pulses (*Figs. 1 & 2; Column 4, Line 22 - Column 5, Line 42*).

Regarding claim 70, ***Hirai*** discloses said horizontal shift register circuit has sampling switches [*Fig. 2, FF1-FF80*], a level shifter [*Fig. 1, 23*], a data latch circuit [*Fig. 1, 22*], and a digital/analog converting circuit [*Fig. 1, 22*] (*Column 4, Line 22 - Column 5, Line 42*).

Should it be shown that ***Hirai*** neglects teaching a digital/analog converting circuit with sufficient specificity; the examiner takes official notice that it would have been obvious to an artisan to incorporate digital/analog converting circuitry, so as to assure that all signals are at appropriate levels.

Claim Rejections - 35 USC § 112

To simplify the issues for appeal (as well as brevity's sake), the examiner has withdrawn some of the rejections under 35 U.S.C. 112, second paragraph.

10. Claims 26-29, 31, 37, 43-48, and 71-78 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results for the claimed subject matter: "***a display***" (*in line 1 of each dependent claim*).

It would be unclear to one having ordinary skill in the art whether "***a display***" in each respective dependent claim is intended to refer back to the earlier claimed "***a liquid crystal display***" (*in independent claim 25, line 1*); or rather whether "***a display***" in each respective dependent claim is intended represent a separate and distinct display from the earlier claimed "***a liquid crystal display***" (*in independent claim 25, line 1*).

Does the display of each of the dependent claims even need to be a liquid crystal display? Or can it be any type of display (*e.g., CRT, EL, FET, etc.*)?

11. Claim 31 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results from the claimed subject matter: "***a surplus connecting region that does not contribute to said display portion does not occur on the said display***" (*in line 1*).

It would be unclear to one having ordinary skill in the art whether or not "***a surplus connecting region***" is an element of the claimed invention.

It's further unclear what if anything such a region is intended to be connecting while it's not contributing or occurring.

Claim 31 is therefore considered amenable to two or more plausible claim constructions.

See Ex parte Miyazaki (*BPAI Precedential 19 November 2008*).

12. The term "***does not contribute***" in claim 31, line 2 is a relative term which renders the claim indefinite.

The term "***contribute***" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

One artisan's impression of a "*contribution*" is just as likely to be another artisan's idea of a detriment.

13. Claim 37 recites the limitation "***a de-multiplexed signal potential***" (*in line 3*).

There is insufficient antecedent basis for this limitation in the claim.

It would be unclear to one having ordinary skill whether or not a de-multiplexer is a claim element.

14. Claims 67-70 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results for the claimed subject matter: "***a display***" (*in line 1 of each dependent claim*).

It would be unclear to one having ordinary skill in the art whether "***a display***" in each respective dependent claim is intended to refer back to the earlier claimed "***a liquid crystal display***" (*in independent claim 49, line 1*); or rather whether "***a display***" in each respective dependent claim is intended represent a separate and distinct display from the earlier claimed "***a liquid crystal display***" (*in independent claim 49, line 1*).

Does the display of each of the dependent claims even need to be a liquid crystal display? Or can it be any type of display (*e.g., CRT, EL, FET, etc.*)?

15. Claim 76 recites the limitation "***digital data boosted***" (*in line 2*). There is insufficient antecedent basis for this limitation in the claim.

It would be unclear to an artisan whether or not a pre-boosted data element is part of the claimed invention.

16. Claim 76 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results from the claimed subject matter: "***digital data boosted by said general driver level shifter by an amount of one horizontal period***" (*in line 2*).

It would be unclear to one having ordinary skill in the art how a time period is even capable of "*boosting*" digital data.

Digital data by it's very definition can only take one of two values.

(10) Response to Argument

To simplify the issues for appeal (as well as brevity's sake), the examiner has withdrawn some of the rejections under 35 U.S.C. 112, second paragraph.

The Appellant states, "*Claims 25-29, 31, 37, 43-47, 71-78 stand or fall together*" (page 19), "*Claim 48 stands or falls alone*" (page 27), and "*Claims 49-70 stand or fall together*" (page 28).

The examiner respectfully notes some of the most seemingly indefinite subject matter is present in the dependent claims -- which stand or fall together with both independent claims 25 and 49.

The Conferees of this brief requested the examiner point out to the Board that independent claim 49 is considered broader in scope than independent claim 25.

Regarding independent claim 25, it is the examiner's opinion that claim 25 is claiming little more than a display having two or more driver circuits (*one driver circuit having more outputs than another*).

It is further the examiner's contention that such a broad claim would read on most any display having five or more line drivers -- which can be arbitrarily combined (*by little more than a labeling convention*) into two or more driver groups/circuits (*with one driver group/circuit having more outputs than another*), as instantly claimed.

Regarding dependent claim 49, the Appellant argues that two prior art references neglect expressly teaching "*transparent insulating substrate*" (*e.g., glass*) subject matter that the instant application itself discloses is conventional in the art of liquid crystal display panels (*see page 1, line 20 of the instant specification*).

Regarding independent claim 49, it is the examiner's opinion that claim 49 is claiming little more than a display having two or more driver circuits (*both driver circuits having the same number of outputs*).

It is further the examiner's contention that such a broad claim would read on most any display having four or more single line drivers -- which can be arbitrarily combined (*by little more than a labeling convention*) into two or more driver circuit pairs/groups (*with each driver circuit pair/group having the same number of outputs*), as instantly claimed.

Claim Rejections - 35 USC § 112

The Appellant argues, "*Claim 25 is drawn to a liquid crystal display comprising: A DISPLAY PORTION, said display portion having a plurality of gate lines... As shown by the uppercase lettering, the a proper antecedent basis has been established within claim 25*" (see pages 10-11 of the brief).

Claims 26-29, 31, 37, 43-48, and 71-78 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of

elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results for the claimed subject matter: "***a display***" (*in line 1 of each dependent claim*).

It would be unclear to one having ordinary skill in the art whether "***a display***" in each respective dependent claim is intended to refer back to the earlier claimed "***a liquid crystal display***" (*in independent claim 25, line 1*); or rather whether "***a display***" in each respective dependent claim is intended represent a separate and distinct display from the earlier claimed "***a liquid crystal display***" (*in independent claim 25, line 1*).

Does the display of each of the dependent claims even need to be a liquid crystal display? Or can it be any type of display (*e.g., CRT, EL, FET, etc.*)?

> The Appellant argues, "*Claim 31 is drawn to a display according to claim 25, wherein A SURPLUS CONNECTING REGION that does not contribute to said display portion does not occur on the said display. For claim construction purposes, the description may act as a sort of dictionary, which explains the invention and may define terms used in the claims. General Electric Co. v. Nintendo Co., 50 USPQ2d 1910, 1914 (Fed. Cir. 1999). Attention is drawn to specification page 16, lines 22-24*" (see page 12 of the brief).

Claim 31 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results from the claimed subject matter: "***a surplus connecting region that does not contribute to said display portion does not occur on the said display***" (*in line 1*).

It would be unclear to one having ordinary skill in the art whether or not "***a surplus connecting region***" is an element of the claimed invention.

It's further unclear what if anything such a region is intended to be connecting while it's not contributing or occurring.

Claim 31 is therefore considered amenable to two or more plausible claim constructions.

See Ex parte Miyazaki (*BPAI Precedential 19 November 2008*).

The term "***does not contribute***" in claim 31, line 2 is a relative term which renders the claim indefinite.

The term "***contribute***" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

One artisan's impression of a "*contribution*" is just as likely to be another artisan's idea of a detriment.

The Appellant argues, "*Claim 37 is drawn to a display according to claim 25, wherein an output terminal of said plurality of driver circuits is electrically connected to an input terminal of a time-divisional switch, said time-divisional switch providing a de-multiplexed signal potential to said signal line, said de- multiplexed signal potential being a signal potential for one of A PLURALITY OF PRIMARY COLORS that is time-divided from another signal potential for*

another of said plurality of primary colors and supplied to said signal line. As shown by the uppercase lettering, the a proper antecedent basis for the terms found within claim 37 has been established within claim 25." (see page 12 of the brief).

Claim 37 recites the limitation "***a de-multiplexed signal potential***" (*in line 3*). There is insufficient antecedent basis for this limitation in the claim.

It would be unclear to one having ordinary skill whether or not a de-multiplexer is a claim element.

The Appellant argues, "*Claim 49 is drawn to a liquid crystal display comprising: A DISPLAY PORTION, said display portion having a plurality of gate lines...*" (see page 14 of the brief).

Claims 67-70 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results for the claimed subject matter: "***a display***" (*in line 1 of each dependent claim*).

It would be unclear to one having ordinary skill in the art whether "***a display***" in each respective dependent claim is intended to refer back to the earlier claimed "***a liquid crystal display***" (*in independent claim 49, line 1*); or rather whether "***a display***" in each respective dependent claim is intended represent a separate and distinct display from the earlier claimed "***a liquid crystal display***" (*in independent claim 49, line 1*).

Does the display of each of the dependent claims even need to be a liquid crystal display? Or can it be any type of display (*e.g., CRT, EL, FET, etc.*)?

> The Appellant argues, "*Claim 76 is drawn to a display according to claim 73, wherein said general driver data latch circuit is a memory to accumulate DIGITAL DA TA boosted by said general driver level shifter by an amount of one horizontal period. Attention is drawn to specification figure 4 and page 11, line 24 to page 12, line 24*" (see page 17 of the brief).

Claim 76 recites the limitation "***digital data boosted***" (*in line 2*). There is insufficient antecedent basis for this limitation in the claim.

It would be unclear to an artisan whether or not a pre-boosted data element is part of the claimed invention.

Claim 76 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results from the claimed subject matter: "***digital data boosted by said general driver level shifter by an amount of one horizontal period***" (*in line 2*).

It would be unclear to one having ordinary skill in the art how a time period is even capable of "*boosting*" digital data.

Digital data by it's very definition can only take one of two values.

Claim Rejections - 35 USC § 102 / 103

"Claims 25-29, 31, 37, 43-47, 71-78 stand or fall together" **(page 19)**

Claims 25-29, 31, 37, 43-48, and 71-78 are rejected under 35 U.S.C. 102(b) as anticipated by ***Takeda et al (US 4,825,203 A)***.

Claims 25-29, 31, 37, 43-48, and 71-78 are rejected under 35 U.S.C. 102(b) as anticipated by ***Hirai (US 5,440,304 A)***.

In the alternative, claims 25-29, 31, 37, 43-48, and 71-78 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Takeda et al (US 4,825,203 A)*** in view of ***Hirai (US 5,440,304 A)***.

Takeda

The Appellant argues, "***Takeda*** *fails to disclose, teach, or suggest a plurality of driver circuits, said plurality of driver circuits including at least one general driver circuit and one remainder driver circuit.*" (see page 23 of the brief).

Takeda discloses a plurality of driver circuits (*wherein the total column electrode drive circuit [Fig. 2: 13] is made up by a plurality of single column driver circuits, each single column driver circuit comprising:*

a shift register [Fig. 1(A): 31],

an output terminal [Fig. 1(A): q],

three AND gate circuits [Fig. 1(A): 37],

three analog switches [Fig. 1(A): 32],

a first condenser [Fig. 1(A): 33],

another analog switch [Fig. 1(A): 34],

a second condenser [Fig. 1(A): 35],

an output buffer [Fig. 1(A): 36], and

a column electrode output terminal [Fig. 1(A): Q]),

said plurality of driver circuits including

at least one general driver circuit (*e.g., an arbitrary grouping of the first three leftmost column driver circuits [Fig. 1(A): (q_1 to Q_1) + (q_2 to Q_2) + (q_3 to Q_3)]*) and

one remainder driver circuit (*e.g., an arbitrary grouping of the last two rightmost column driver circuits [Fig. 1(A): (q_{N-1} to Q_{N-1}) + (q_N to Q_N)]*).

The Appellant argues, "***Takeda*** *fails to disclose, teach, or suggest each said at least one general driver circuit having a general driver horizontal shift register circuit and a plurality of general driver circuit output terminals, a general driver circuit output terminal of said plurality of general driver circuit output terminals providing a signal potential to one of said plurality of signal lines.*" (see page 24 of the brief).

Takeda discloses each said at least one general driver circuit having

a general driver horizontal shift register circuit [*Fig. 1(A): shift register 31 at output terminals* $q_{1\text{-}3}$] and

a plurality of general driver circuit output terminals [*Fig. 1(A): output terminals* $Q_{1\text{-}3}$ *from output buffers* $36_{1\text{-}3}$],

a general driver circuit output terminal of said plurality of general driver circuit output terminals providing a signal potential ("*a signal corresponding to the display pattern*") to one of said plurality of signal lines (*wherein output terminals [Fig. 1(A):* $Q_{1\text{-}3}$*] from output buffers [Fig. 1(A):* $36_{1\text{-}3}$*] output display signals to the first three leftmost column electrode lines [Fig. 2: column electrodes 11-b]).*

The Appellant argues, "***Takeda*** *fails to disclose, teach, or suggest said remainder driver circuit having a remainder driver horizontal shift register circuit and a plurality of remainder driver circuit output terminals, a remainder driver circuit output terminal of said plurality of remainder driver circuit output terminals providing another signal potential to another of said plurality of signal lines*" (see page 24 of the brief).

Takeda discloses said remainder driver circuit having

a remainder driver horizontal shift register circuit [*Fig. 1(A): shift register 31 at output terminals q_{N-1}, q_N*] and

a plurality of remainder driver circuit output terminals [*Fig. 1(A): output terminals Q_{N-1}, Q_N from output buffers 36_{N-1}, 36_N*],

a remainder driver circuit output terminal of said plurality of remainder driver circuit output terminals providing another signal potential to another of said plurality of signal lines (*wherein output terminals [Fig. 1(A): Q_{N-1}, Q_N] from output buffers [Fig. 1(A): 36_{N-1}, 36_N] output display signals to the last two rightmost column electrode lines [Fig. 2: column electrodes 11-b])*.

The Appellant argues, "***Takeda*** *fails to disclose, teach, or suggest the quantity of said remainder driver circuit output terminals being defined as (S- (OP * (DC-1))), "S" being the quantity of said plurality of signal lines, "OP" being the quantity of said general driver circuit output terminals, and "DC" being the quantity of said plurality of driver circuits, and said quantity of said general driver circuit output terminals being different than said quantity of said remainder driver circuit output terminals*" (see pages 24-25 of the brief).

Takeda discloses the quantity [*2*] of said remainder driver circuit output terminals [*Fig. 1(A): output terminals Q_{N-1}, Q_N*] being defined as (S - (OP * (DC-1))),

"S" being the quantity [*5*] of said plurality of signal lines [*Fig. 1(A):For simplicity's sake set the number of column signal lines at N = 5. However please note, the number of column*

signal lines could be set as high as desired. Simply increase the number of general driver circuit output terminals accordingly and the instantly claimed equation will still work.],

"OP" being the quantity [*3*] of said general driver circuit output terminals [*Fig. 1(A): output terminals Q_{1-3}*], and

"DC" being the quantity [*2*] of said plurality of driver circuits [*Fig. 1(A): output terminals Q_{N-1}, Q_N*], and

said quantity [*3*] of said general driver circuit output terminals being different than said quantity [*2*] of said remainder driver circuit output terminals [*Fig. 1(A) and Column 4, Lines 22-68. Wherein S - (OP * (DC-1)) = 5 - (3 * (2-1)) = 5 - (3 * 1) = 5 - 3 = 2 = the quantity of remainder driver circuit output terminals = 2*].

Hirai

The Appellant argues, "***Hirai*** *fails to disclose, teach, or suggest the quantity of said remainder driver circuit output terminals being defined as (S- (OP * (DC-1))), "S" being the quantity of said plurality of signal lines, "OP" being the quantity of said general driver circuit output terminals, and "DC" being the quantity of said plurality of driver circuits, and said quantity of said general driver circuit output terminals being different than said quantity of said remainder driver circuit output terminals*" (see page 27 of the brief).

Hirai discloses the quantity [*16*] of said remainder driver circuit output terminals [*Fig. 5: Y_1-Y_{16}*] being defined as (S - (OP * (DC-1))),

"S" being the quantity [*176*] of said plurality of signal lines [*Fig. 5:* $(Y_1\text{-}Y_{80}) + (Y_1\text{-}Y_{80}) + (Y_1\text{-}Y_{16}) = Y_{176}$],

"OP" being the quantity [*80*] of said general driver circuit output terminals [*Fig. 5:* $Y_1\text{-}Y_{80}$], and

"DC" being the quantity [*3*] of said plurality of driver circuits [*Fig. 5: two leftmost general driver circuits and one rightmost remainder driver circuit = three driver circuits total*] , and

said quantity [*80*] of said general driver circuit output terminals being different than said quantity [*16*] of said remainder driver circuit output terminals (*Column 1, Line 5 - Column 2, Line 60*).

Additionally, it would have been obvious to an artisan to combine ***Hirai's*** 80-pin output drivers [*Fig. 5:* $Y_1\text{-}Y_{80}$] with ***Takeda's*** N-pin output drivers [*Fig. 1(A):* $Q_1\text{-}Q_N$], so as to provide a total number of output pins equaling the total number of display signal lines -- resulting in the instantly claimed invention in every incarnation where ***Takeda's*** *N* does not also equal 80.

"*Claim 48 stands or falls alone*" (page 27)

Takeda / Hirai

The Appellant argues, "***Takeda*** *and* ***Hirai****, either individually or as a whole, fail to disclose, teach or suggest the presence of a transparent insulating substrate*" (see page 27 of the brief).

Takeda discloses said plurality of driver circuits are driver integrated circuits arranged in an outside of a transparent insulating substrate on which said display portion is formed (*Fig. 2; Column 2, Line 56 - Column 4, Line 6*).

Takeda states, "*FIG. 2 is a block diagram which explains a general configuration of the liquid crystal color display device used in this invention. Numeral (11) in the figure is the liquid crystal color display panel. Switching transistors 11-d are built into the display picture elements 11-c, which are the intersecting points of the row electrodes 11-a and column electrodes 11-b on one of the circuit boards of the panel (11). On the other circuit board, there are counter electrodes, and respective color filters: red (R), green (G) and blue (B) opposing the display picture elements, arranged, for example, as shown in the diagram*" (Column 2, Lines 56-68).

As such at least one of ***Takeda's*** circuit boards would necessarily, inherently, and obviously be both "*transparent*" and "*insulating*." If neither of the circuit boards was transparent, it would not be possible to see ***Takeda's*** pixels, thereby preventing ***Takeda's*** invention from being "*a display*."

Moreover, circuit boards are by, definition, "*insulating*." For example: Random House Dictionary defines "*circuit board*" as "*a sheet of insulating material used for the mounting and interconnection (often by a printed circuit) of components in electronic equipment*."

Additionally, ***Takeda's*** disclosed color filters and twisted nematic liquid crystal layer would both constitute "*a transparent insulating substrate*," as instantly claimed.

Hirai also discloses said plurality of driver circuits are driver integrated circuits arranged in an outside of a transparent insulating substrate on which said display portion is formed (*Fig. 5; Column 1, Line 5 - Column 2, Line 60*).

Here too, ***Hirai's*** disclosed liquid crystal layer would both constitute "*a transparent insulating substrate*," as instantly claimed.

Finally, it would have been obvious to one having ordinary skill in the art at the time of invention to form a display portion on a transparent insulating substrate (*such as glass*), as is customary and conventional in the field of liquid crystal displays (*as is acknowledged in on the very first page of the instant application's specification -- see page 1, line 20*).

"*Claims 49-70 stand or fall together*" (page 28)

Claims 49-66 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Takeda et al (US 4,825,203 A)*** in view of ***Lee (US 5,426,447 A)***.

Claims 67-70 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Takeda et al (US 4,825,203 A)*** and ***Lee (US 5,426,447 A)*** as applied to *claim 49* above, and further in view of ***Hirai (US 5,440,304 A)***.

Claim 49 is rejected under 35 U.S.C. 102(b) as being anticipated by ***Hayashi et al (US 4,745,406 A)***.

Claims 67-70 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Hayashi et al (US 4,745,406 A)*** in view of ***Hirai (US 5,440,304 A)***.

Claims 67-70 are rejected under 35 U.S.C. 102(b) as anticipated by ***Hirai (US 5,440,304 A)***.

Or, in the alternative, claims 67-70 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Hirai (US 5,440,304 A)***.

Takeda

The Appellant argues, "***Takeda*** *fails to disclose, teach, or suggest a plurality of driver circuits, said plurality of driver circuits including at least one general driver circuit and one remainder driver circuit*" (see page 32 of the brief).

In response to applicant's argument that the reference(s) fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., *a plurality of driver circuits, said plurality of driver circuits including at least one general driver circuit and one remainder driver circuit*) are not recited in the rejected claims 49-70.

Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Takeda discloses a plurality of driver circuits (*wherein the total column electrode drive circuit [Fig. 2: 13] is made up by a plurality of single column driver circuits, each single column driver circuit comprising:*

a shift register [Fig. 1(A): 31],

an output terminal [Fig. 1(A): q],

three AND gate circuits [Fig. 1(A): 37],

three analog switches [Fig. 1(A): 32],

a first condenser [Fig. 1(A): 33],

another analog switch [Fig. 1(A): 34],

a second condenser [Fig. 1(A): 35],

an output buffer [Fig. 1(A): 36], and

a column electrode output terminal [Fig. 1(A): Q]) (*see Column 2, Line 56 - Column 3, Line 27*),

each of said plurality of driver circuits having a plurality of driver circuit output terminals (*e.g., an arbitrary pairing of every two adjacent column driver circuits [Fig. 1(A): ($q_{1\text{-}2}$ to $Q_{1\text{-}2}$), ($q_{3\text{-}4}$ to $Q_{3\text{-}4}$), ... , ($q_{N\text{-}1,\,N}$ to $Q_{N\text{-}1,\,N}$)]*),

a driver circuit output terminal [*Fig. 1(A): output terminals $Q_{1\text{-}2}$ from output buffers $36_{1\text{-}2}$; output terminals $Q_{3\text{-}4}$ from output buffers $36_{3\text{-}4}$; ... ; and output terminals $Q_{N\text{-}1,\,N}$ from output buffers $36_{N\text{-}1,\,N}$*] of said a plurality of driver circuit output terminals providing a signal potential ("*a signal corresponding to the display pattern*") to a signal line of said plurality of signal lines (*wherein output terminals [Fig. 1(A): $Q_{1\text{-}N}$] from output buffers [Fig. 1(A): $36_{1\text{-}N}$] output display signals to the corresponding column electrode lines [Fig. 2: column electrodes 11-b]).*

The Appellant argues, "***Takeda*** *fails to disclose, teach, or suggest the quantity of said driver circuit output terminals being the same quantity for said each of said plurality of driver circuits*" (see page 32 of the brief).

Takeda discloses the quantity [*2*] of said driver circuit output terminals [*Fig. 1(A): two output terminals for each of:* Q_{1-2}; Q_{3-4}; $Q_{N-1, N}$] being the same quantity for said each of said plurality of driver circuits.

The Appellant argues, "***Takeda*** *fails to disclose, teach, or suggest the quantity of said driver circuits being defined as N/n, wherein "N" is the quantity of said signal lines and "n" is said quantity of said driver circuit output terminals*" (see page 32 of the brief).

Takeda discloses the quantity of said driver circuits being defined as N/n [$N / n = 6 / 2 =$ *3 driver circuits : first driver circuit (*q_{1-2} *to* Q_{1-2}*), second driver circuit (*q_{3-4} *to* Q_{3-4}*), and third driver circuit (*q_{5-6} *to* Q_{5-6}*)*], wherein

"N" is the quantity [*Fig. 1(A): e.g., for simplicity's sake arbitrarily set N = 6 column signal lines. However please note, the number of column signal lines could be set as high as desired. Simply increase the number of driver circuits accordingly and the instantly claimed equation will still work.*] of said signal lines and

"n" is said quantity [*2*] of said driver circuit output terminals [*Fig. 1(A): two output terminals for each of:* Q_{1-2}; Q_{3-4}; $Q_{N-1, N}$] (*Column 4, Lines 22-68*).

Lee

The Appellant argues, "***Lee*** *fails to disclose, teach, or suggest a plurality of driver circuits, said plurality of driver circuits including at least one general driver circuit and one remainder driver circuit*" (see page 34 of the brief).

In response to applicant's argument that the reference(s) fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., *a plurality of driver circuits, said plurality of driver circuits including at least one general driver circuit and one remainder driver circuit*) are not recited in the rejected claims 49-70.

Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

The Appellant argues, "***Lee*** *fails to disclose, teach, or suggest the quantity of said driver circuit output terminals being the same quantity for said each of said plurality of driver circuits*" (see page 34 of the brief).

The Appellant argues, "***Lee*** *fails to disclose, teach, or suggest the quantity of said driver circuits being defined as N/n, wherein "N" is the quantity of said signal lines and "n" is said quantity of said driver circuit output terminals*" (see page 34 of the brief).

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

The examiner does not argue now nor in the final Office action that ***Lee*** teaches such subject matter (*as argued by the Appellant on page 34 of the brief*).

Lee discloses a transparent insulating substrate (*e.g. glass*) on which a display portion comprising a plurality of "*pixels*" is formed (*Column 1, Lines 18-30*).

Hirai

The Appellant argues, "***Hirai*** *fails to disclose, teach, or suggest a plurality of driver circuits, said plurality of driver circuits including at least one general driver circuit and one remainder driver circuit*" (see page 36 of the brief).

In response to applicant's argument that the reference(s) fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., *a plurality of*

driver circuits, said plurality of driver circuits including at least one general driver circuit and one remainder driver circuit) are not recited in the rejected claims 49-70.

Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Hirai discloses a plurality of driver circuits [*Fig. 4: 20*],

each of said plurality of driver circuits [*Fig. 5: first driver circuit Y_1-Y_{72}; second driver circuit Y_{73}-Y_{144}; and third driver circuit Y_{145}-Y_{216}*] having a plurality of driver circuit output terminals [*Fig. 4: Y_1-Y_{72}*],

a driver circuit output terminal of said a plurality of driver circuit output terminals providing a signal potential to a signal line of said plurality of signal lines.

The Appellant argues, "***Hirai*** *fails to disclose, teach, or suggest the quantity of said driver circuit output terminals being the same quantity for said each of said plurality of driver circuits*" (see page 36 of the brief).

Hirai discloses the quantity [*Fig. 4: 72*] of said driver circuit output terminals [*Fig. 4: Y_1-Y_{72}*] being the same quantity for said each of said plurality of driver circuits (*see Fig. 4*).

The Appellant argues, "***Hirai*** *fails to disclose, teach, or suggest the quantity of said driver circuits being defined as N/n, wherein "N" is the quantity of said signal lines and "n" is said quantity of said driver circuit output terminals*" (see page 37 of the brief).

Hirai discloses the quantity of said driver circuits being defined as N/n [$N / n = 216 / 72 = 3$ *driver circuits: first driver circuit* Y_1-Y_{72}*; second driver circuit* Y_{73}-Y_{144}*; and third driver circuit* Y_{145}-Y_{216}] , wherein

"N" is the quantity of said signal lines [$N = 72 + 72 + 72 = 216$] and

"n" is said quantity [$n = 72$] of said driver circuit output terminals [*Fig. 4:* Y_1-Y_{72}];

wherein

said each of said plurality of driver circuits has a horizontal shift register circuit [*Figs. 1 & 2; 11 and Fig. 3; 21*] (*Column 4, Line 15 - Column 5, Line 42*).

Additionally, it would have been obvious to an artisan to combine ***Hirai's*** 80-pin output drivers [*Fig. 5:* Y_1-Y_{80}], or alternately ***Hirai's*** 72-pin output drivers [*Fig. 4:* Y_1-Y_{72}], with ***Takeda's*** N-pin output drivers [*Fig. 1(A):* Q_1-Q_N], so as to provide a total number of output pins equaling the total number of display signal lines -- resulting in the instantly claimed invention in every incarnation where ***Takeda's*** *N* also equals 80, or alternately 72.

Hayashi

The Appellant argues, "***Hayashi*** *fails to disclose, teach, or suggest a plurality of driver circuits, said plurality of driver circuits including at least one general driver circuit and one remainder driver circuit*" (see page 38 of the brief).

In response to applicant's argument that the reference(s) fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., *a plurality of driver circuits, said plurality of driver circuits including at least one general driver circuit and one remainder driver circuit*) are not recited in the rejected claims 49-70.

Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Hayashi discloses a plurality of driver circuits [*Fig. 8: "the first driver circuit" = (M_1 and M_2) and "the second driver circuit" = (M_3 and M_4)*],

each of said plurality of driver circuits having a plurality of driver circuit output terminals [*Fig. 8: "the first driver circuit" = (M_1 and M_2) has two output terminals driving the first two column electrodes and "the second driver circuit" = (M_3 and M_4) has two output terminals driving the second two column electrodes*],

a driver circuit output terminal of said a plurality of driver circuit output terminals providing a signal potential to a signal line of said plurality of signal lines.

The Appellant argues, "***Hayashi*** *fails to disclose, teach, or suggest the quantity of said driver circuit output terminals being the same quantity for said each of said plurality of driver circuits*" (see page 38 of the brief).

Hayashi discloses the quantity [*2*] of said driver circuit output terminals being the same quantity for said each of said plurality of driver circuits [*Fig. 8: "the first driver circuit" = (M_1 and M_2) has two output terminals driving the first two column electrodes and "the second driver circuit" = (M_3 and M_4) has two output terminals driving the second two column electrodes*].

The Appellant argues, "***Hayashi*** *fails to disclose, teach, or suggest the quantity of said driver circuits being defined as N/n, wherein "N" is the quantity of said signal lines and "n" is said quantity of said driver circuit output terminals*" (see page 38 of the brief).

Hayashi discloses the quantity of said driver circuits being defined as N/n [*$N / n = 4 / 2 = 2$ driver circuits: Fig. 8: "the first driver circuit" = (M_1 and M_2) and "the second driver circuit" = (M_3 and M_4)*] , wherein

"N" is the quantity [*4*] of said signal lines [*Fig. 8: Columns 1-4*] and

"n" is said quantity [*2*] of said driver circuit output terminals [*Fig. 8: "the first driver circuit" = (M_1 and M_2) has two output terminals driving the first two column electrodes and "the second driver circuit" = (M_3 and M_4) has two output terminals driving the second two column electrodes*] (*Column 4, Line 43 - Column 5, Line 8*).

Additionally, it would have been obvious to an artisan to combine ***Hirai's*** 80-pin output drivers [*Fig. 5:* Y_1-Y_{80}], or alternately ***Hirai's*** 72-pin output drivers [*Fig. 4:* Y_1-Y_{72}], with ***Hayashi's*** M_{s+N} pin shift register circuitry [*Fig. 8: 2*], so as to provide a total number of output pins equaling the total number of display signal lines -- resulting in the instantly claimed invention in every incarnation where ***Hayashi's*** *N* also equals 79, or alternately 71.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Jeff Piziali/

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10 April 2009

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